Claims

[c1] 1. An electronic device comprising:
a semiconductor device comprising:
a pass gate transistor including a first fin body and a first gate, said first fin body having opposing sidewalls, each sidewall aligned in a first direction having a first majority carrier mobility, said first gate adjacent to both sidewalls of said first fin body;
a pull down latch transistor including a second fin body and a second gate, said second fin body having opposing sidewalls, each sidewall aligned in a second direction having a second majority carrier mobility, said second gate adjacent to both sidewalls of said second fin body;
a pull up latch transistor including a third fin body and a third gate, said third fin body having opposing sidewalls, each sidewall aligned in a third direction having a first majority carrier mobility, said third gate adjacent to both sidewalls of said third fin body;
wherein all of said first, second and third directions are not the same direction; and
one or more CMOS chevron logic circuits, crystal planes of bodies of transistors of said CMOS chevron logic circuits and crystal planes of said first, second and third fin

bodies co-aligned.

[c2] 2. The semiconductor device of claim 1, wherein said first and second directions are parallel to a {100} crystal plane of said fin bodies and said second direction is aligned between said {100} crystal plane and a {110} crystal plane of said fin bodies.

[c3] 3. The semiconductor device of claim 2, wherein said second direction is halfway between said {100} crystal plane and said {110} crystal plane.

[c4] 4. The semiconductor device of claim 1, wherein said first majority carrier mobility is a high majority carrier mobility, said second majority carrier mobility is a high majority carrier mobility and said third majority carrier mobility is a medium majority carrier mobility.

[c5] 5. The semiconductor device of claim 1, wherein said second direction is parallel to a {100} crystal plane of said fin bodies and said first and third directions and aligned between said {100} crystal plane and a {110} crystal plane of said fin bodies.

[c6] 6. The semiconductor device of claim 5, wherein said first and third directions are in a same direction which bisects an angle between said {100} crystal plane and said {110} crystal plane.

[c7] 7. The semiconductor device of claim 1, wherein said first majority carrier mobility is a high majority carrier mobility, said second majority carrier mobility is a medium majority carrier mobility and said third majority carrier mobility is a medium majority carrier mobility.

[c8] 8. The semiconductor device of claim 1, wherein said first, second and third directions each bisects an angle between said {100} and a {110} crystal planes of said first, second and third fin bodies respectively.

[c9] 9. The semiconductor device of claim 8, wherein said first, second and third direction are equal and halfway between said {100} crystal plane and said {110} crystal plane.

[c10] 10. The semiconductor device of claim 1, wherein said first majority carrier mobility is a medium majority carrier mobility, said second majority carrier mobility is a medium majority carrier mobility and said third majority carrier mobility is a medium majority carrier mobility.

[c11] 11. The semiconductor device of claim 1, wherein said first fin body and said second fin body are contiguous.

[c12] 12. The semiconductor device of claim 1, wherein said second and third gates are contiguous.

[c13] 13. The semiconductor device of claim 1, wherein:
said first fin body includes two fin portions, each fin portion having opposing sidewalls, said fin portions separated by a gap; and
wherein said first gate is adjacent to both sidewalls of both fin portions.

[c14] 14. The semiconductor device of claim 1, wherein said pass gate transistor and said pull down transistor latch are NFETs and said pull-up latch transistor is a PFET.

[c15] 15. A method of fabricating a semiconductor device comprising:
forming a first fin body of a pass gate transistor from a crystal layer, said first fin body having opposing sidewalls, each sidewall aligned in a first direction having a first majority carrier mobility;
forming a second fin body of a pass gate transistor from said crystal layer, said second fin body having opposing sidewalls, each sidewall aligned in a second direction having a second majority carrier mobility;
forming a third fin body of a pass gate transistor from said crystal layer said third fin body having opposing sidewalls, each sidewall aligned in a first direction having a third majority carrier mobility; and
forming a first gate adjacent to both sidewalls of said

first fin body, a second gate adjacent to both sidewalls of said second fin body and a third gate adjacent to both sidewalls of said third fin body
wherein all of said first, second and third directions are not the same direction; and
forming bodies of CMOS devices of one or more CMOS chevron logic circuits from said crystal layer.

[c16] 16. The method of claim 15, wherein said first and second directions are parallel to a {100} crystal plane of said fin bodies and said second direction is aligned between said {100} crystal plane and a {110} crystal plane of said fin bodies.

[c17] 17. The method of claim 16, wherein said second direction is halfway between said {100} crystal plane and said {110} crystal plane.

[c18] 18. The method device of claim 15, wherein said first majority carrier mobility is a high majority carrier mobility, said second majority carrier mobility is a high majority carrier mobility and said third majority carrier mobility is a medium majority carrier mobility.

[c19] 19. The method of claim 15, wherein said second direction is parallel to a {100} crystal plane of said fin bodies and said first and third directions and aligned between

said {100} crystal plane and a {110} crystal plane of said fin bodies.

[c20] 20. The method of claim 19, wherein said first and third directions are in a same direction which bisects an angle between said {100} crystal plane and said {110} crystal plane.

[c21] 21. The method of claim 15, wherein said first majority carrier mobility is a high majority carrier mobility, said second majority carrier mobility is a medium majority carrier mobility and said third majority carrier mobility is a medium majority carrier mobility.

[c22] 22. The method of claim 15, wherein said first, second and third directions are aligned between said {100} and a {110} crystal planes of said fin bodies.

[c23] 23. The method of claim 22, wherein said first, second and third directions each bisects an angle between said {100} and a {110} crystal planes of said first, second and third fin bodies respectively.

[c24] 24. The method of claim 15, wherein said first majority carrier mobility is a medium majority carrier mobility, said second majority carrier mobility is a medium majority carrier mobility and said third majority carrier mobility is a medium majority carrier mobility.

[c25] 25. The method of claim 15, wherein said first fin body and said second fin body are contiguous.

[c26] 26. The method of claim 15, wherein said second and third gates are contiguous.

[c27] 27. The method of claim 15, wherein:
said first fin body includes two fin portions, each fin portion having opposing sidewalls, said fin portions separated by a gap; and
wherein said first gate is adjacent to both sidewalls of both fin portions.

[c28] 28. The method of claim 15, wherein said pass gate transistor and said pull down latch transistor are NFETs and said pull-up latch transistor is a PFET.

[c29] 29. An electronic device comprising:
an SRAM cell comprising:
first and second pass gate transistors, each pass gate transistor including a fin body and a gate, said first fin bodies each having opposing sidewalls and each sidewall aligned in a first direction having a first majority carrier mobility, said gate adjacent to both sidewalls;
first and second pull down latch transistors, each pull down transistor including a fin body and a gate, each fin body having opposing sidewalls and each sidewall

aligned in a second direction having a second majority carrier mobility, said gate adjacent to both sidewalls;
first and second pull up latch transistors, each latch transistor including a fin body and a gate, each fin body having opposing sidewalls and each sidewall aligned in a third direction having a third majority carrier mobility, said gate adjacent to both sidewalls, said third direction aligned between a {100} crystal plane and a {110} of said fin bodies of said first and second pull up latch transistors; and
wherein all of said first, second and third directions are not the same direction; and
one or more CMOS chevron logic circuits, crystal planes of bodies of transistors of said CMOS chevron logic circuits and crystal planes of said first, second and third fin bodies co-aligned.

[c30] 30. The SRAM cell of claim 29, wherein said first and second directions are aligned with said {100}crystal plane, said first direction is aligned with said {100} crystal plane and said second direction bisects an angle between said {100} and {110} crystal planes, or both said first and second directions each bisect the angle between said {100} and {110} crystal planes.